TSMC-03-360

October 15, 2003

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/618,536 07/11/03

Jeun-Chen Lin et al.

IMPROVED ADHESION OF COPPER AND ETCH STOP LAYER FOR COPPER ALLOY

Grp. Art Unit:

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on October 20, 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 10/20/03

U.S. Patent 6,406,996 to Bernard et al., "Sub-Cap and Method of Manufacture Therefor in Integrated Circuit Capping Layers," discloses copper dual damascene interconnects with sub cap and cap layers.

U.S. Patent 6,169,028 to Wang et al., "Method Fabricating Metal Interconnected Structure," discloses an oxide cap over a copper dual damascene interconnect.

U.S. Patent 6,309,970 to Ito et al., "Method of Forming Multi-Level Copper Interconnect with Formation of Copper Oxide on Exposed Copper Surface," discloses a copper oxide on a copper surface.

U.S. Patent 6,274,499 to Gupta et al., "Method to Avoid Copper Contamination During Copper Etching and CMP," discloses a dielectric cap over an interconnect.

U.S. Patent 6,054,769 to Jeng, "Low Capacitance Interconnect Structures in Integrated Circuits Having an Adhesion and Protective Overlayer for Low Dielectric Materials," discloses a method and structure for integrating polymer and other low dielectric constant materials, which may have undesirable properties, into integrated circuit structures and processes, especially those requiring multiple levels of interconnect lines.

TSMC-02-360

U.S. Patent 6,348,407 to Gupta et al., "Method to Improve Adhesion of Organic Dielectrics in Dual Damascene Interconnects," discusses a method of fabrication used for semiconductor integrated circuit devices.

U.S. Patent 6,365,502 to Paranjpe et al., "Microelectronic Interconnect Material with Adhesion Promotion Layer and Fabrication Method," discusses a microelectronic semiconductor interconnect structure barrier and method of deposition which provides improved conductive barrier material properties for high-performance device interconnects.

TSMC-01-1676, Serial No. 10/361,732, filed on 02/10/03 and TSMC-02-338, Serial No. 10/350,837, filed on 01/24/03, both assigned to common assignee discuss the fabrication of integrated circuit devices.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
TSMC-02-360	10/618,536
Applicant: Jeun-Chen Lin et al.	
Filing Date: 07/11/03	Group Art Unit:

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6406996	6/18/02	Bernard et al.	438	653	9/30/00
	6169028	1/2/01	Wang et al.	438	653	1/26/99
	6309970	10/30/01	Ito et al.	438	687	8/30/99
	6274499	8/14/01	Gupta et al.	438	692	11/19/99
	6054769	4/25/00	Jeng	257	758	1/17/97
	6348407	2/19/02	Gupta et al.	438	637	3/15/01
	6365502	4/2/02	Paranjpe et al.	438	622	3/3/00

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

- TSMC-01-1676, Serial No. 10/361,732, filed on 02/10/03, assigned to common assignee, "Barrier Free Copper Interconnect by Multi-Layer Copper Seed".
- TSMC-02-338, Serial No. 10/350,837, filed on 01/24/03, assigned to common assignee, "Improved Method of Barrier-less Integration with Copper Alloy."

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant